Microfabricated ion trap for a single-ion optical clock

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Single ion trapped optical clock :

Fundamental physics tests

Relativistic geodesy

Deep-space navigation & VLBI

<u>Compact Yb^+ optical atomic clock:</u>

- Ions require smaller set-up than neutral atoms.
- Can be trapped at room temperature.
- Well known metrology for Yb^+.
- Every laser frequencies can be reached with ECDL (for Yb^+).
- Possibility to reach small volume for future industrial application.

<u>Goals:</u>

- Frequency stability $\sigma_y(1s) = 10^{-14}\,\tau^{-1/2}$
- Volume < 500 L
- 10 times better than hydrogen Maser within the same volume.

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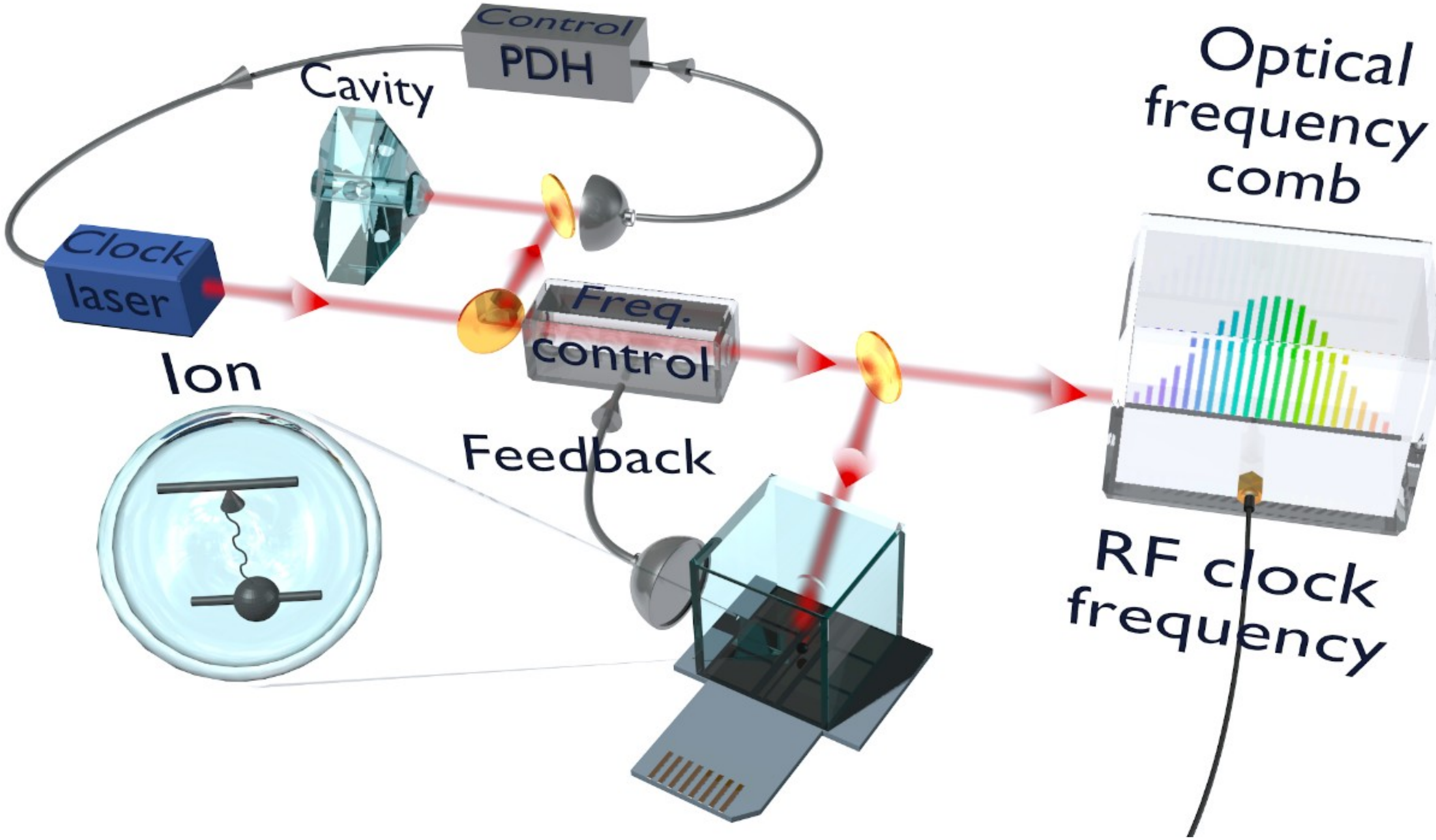
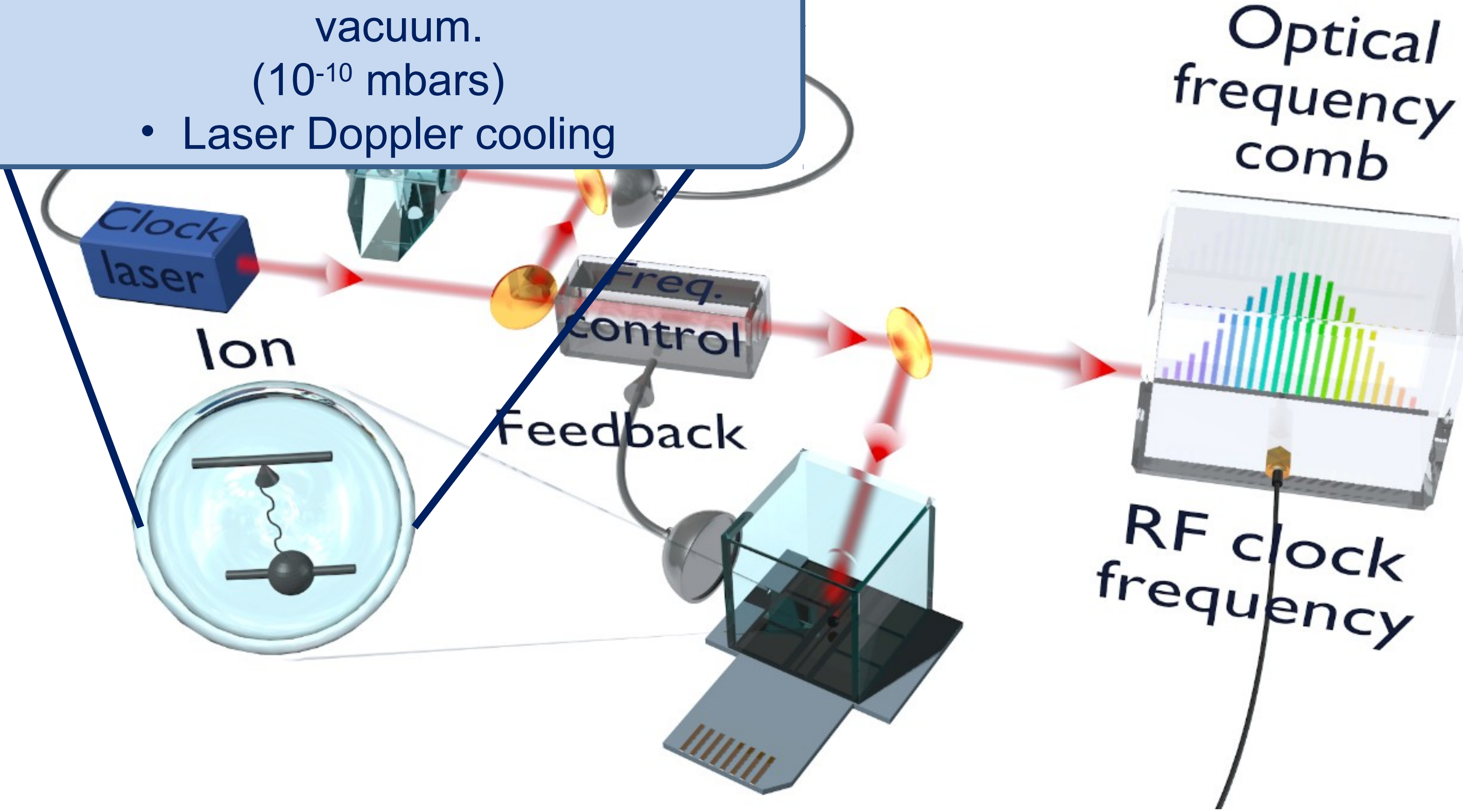
Single ion trapped optical clock

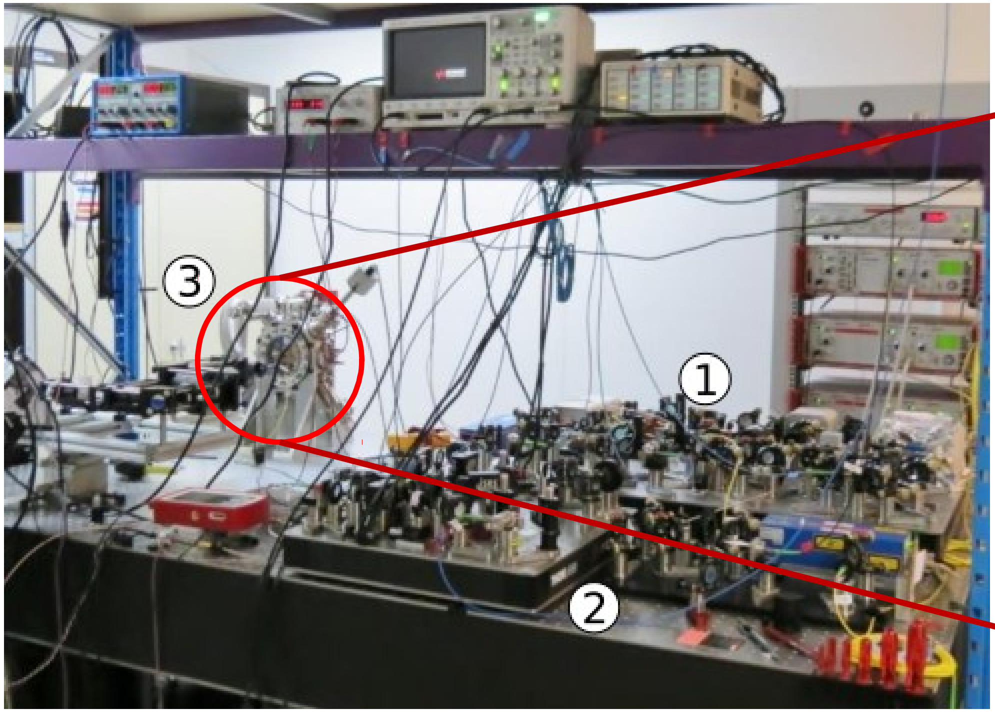


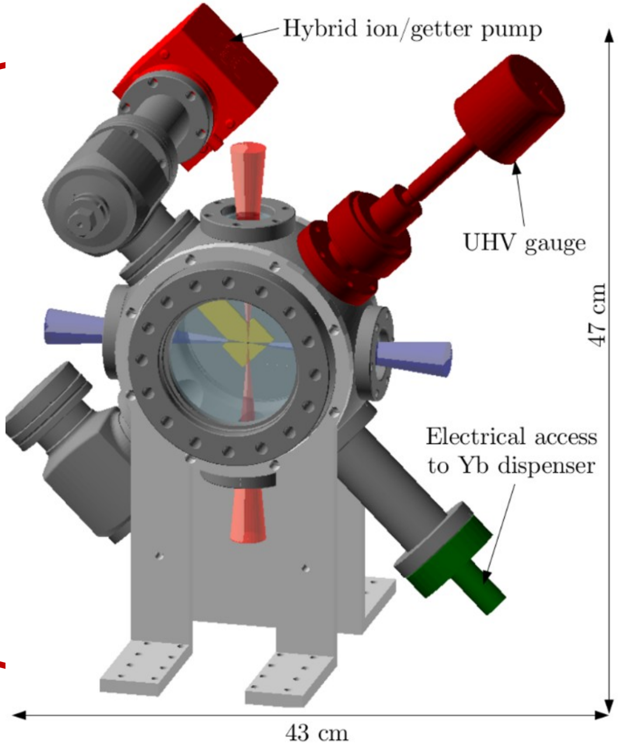
Single ion trapped optical clock

- Ion Yb^+
- Surface Paul trap in ultra-high vacuum. (10^{-10} mbars)
- Laser Doppler cooling



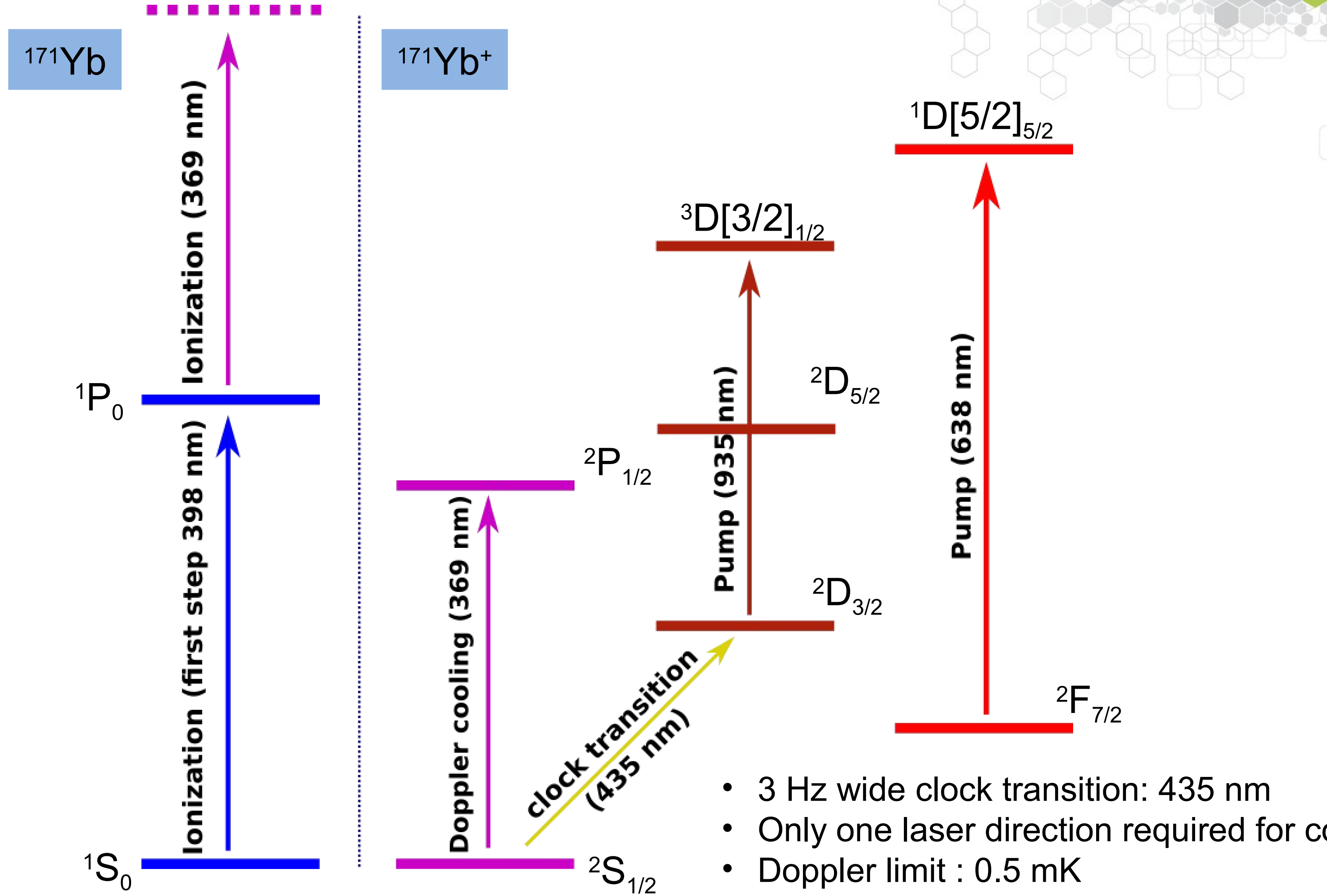
Laser bench





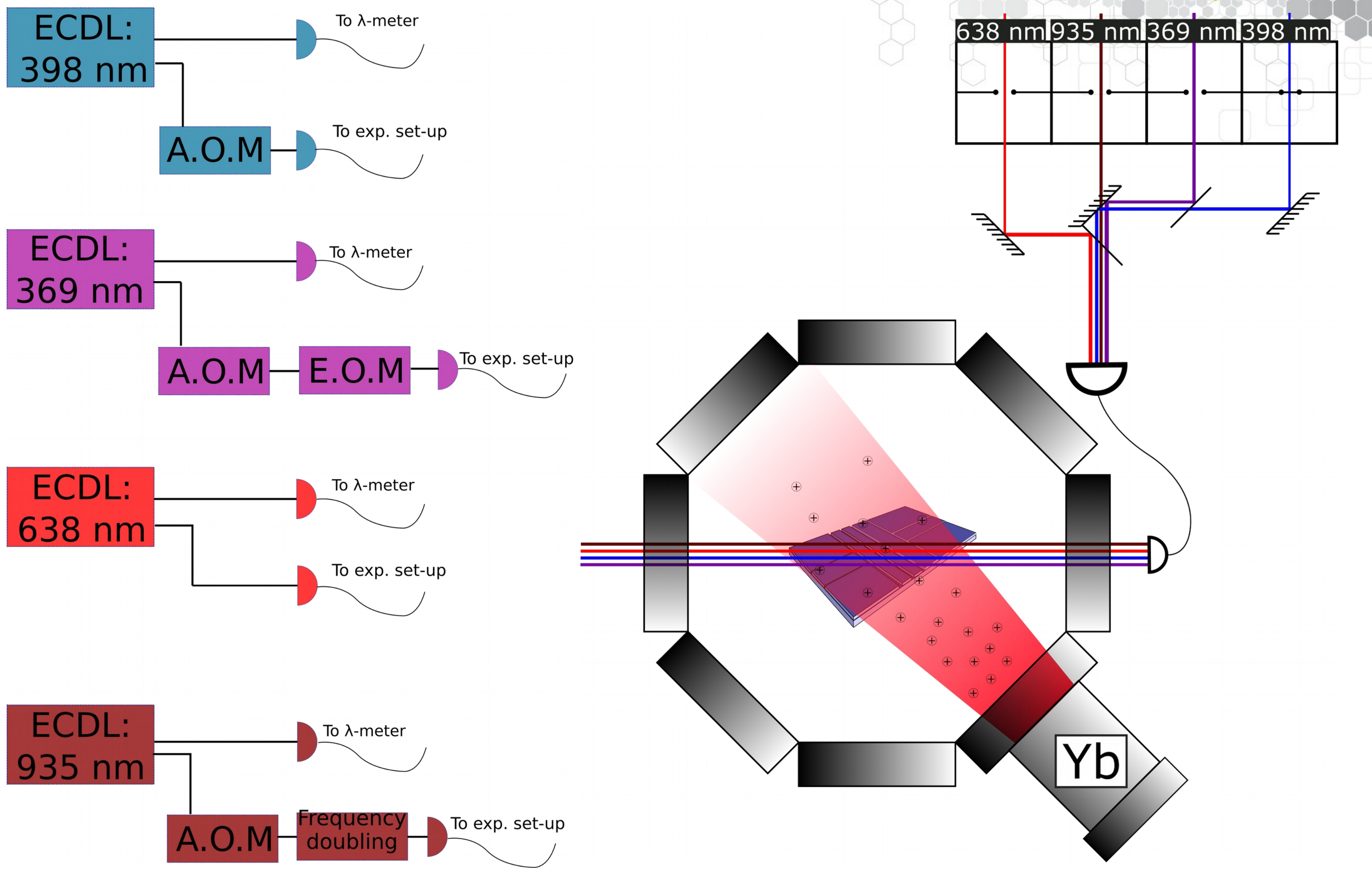
- 1) + 2) Main breadboard + recoupling breadboard
- 3) Main chamber + detection set-up.

Yb+ energy levels



- 3 Hz wide clock transition: 435 nm
- Only one laser direction required for cooling
- Doppler limit : 0.5 mK
- Secondary clock transition: 467 nm

Lasers set-up

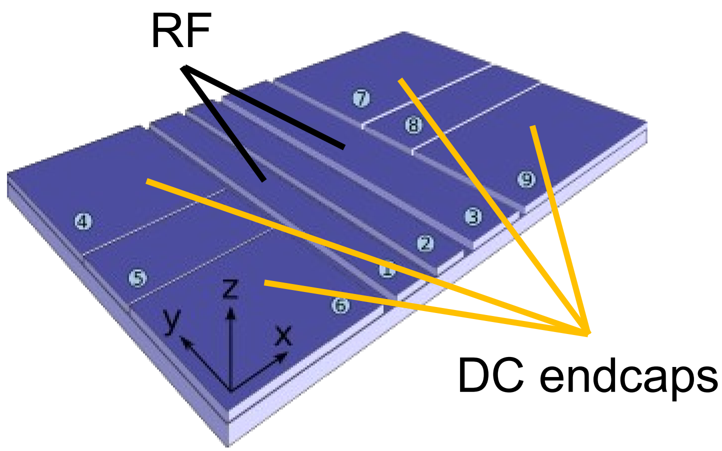


Surface Paul trap

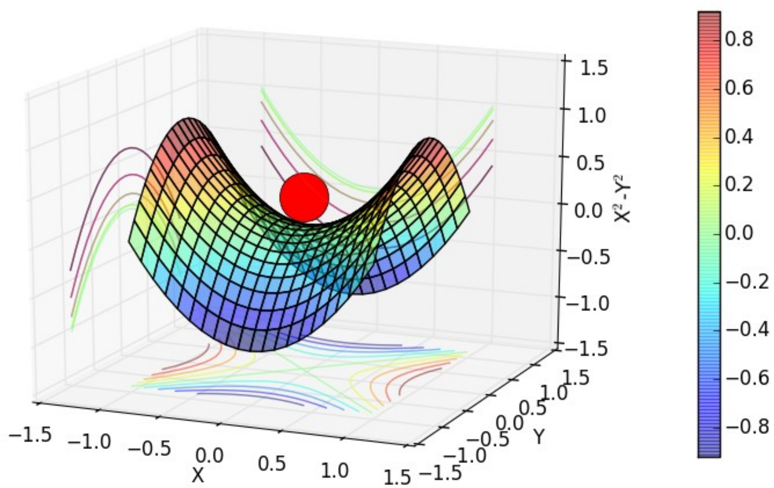
- Surface Paul trap.
- RF potential
- Two RF electrodes
- DC endcaps and control electrodes

- Distance ion – trap surface proportional to central electrode width → broad one.

- Anomalous heating : mecanism of ion heating which grow as $1/r^4$. (r : distance ion - trap surface).

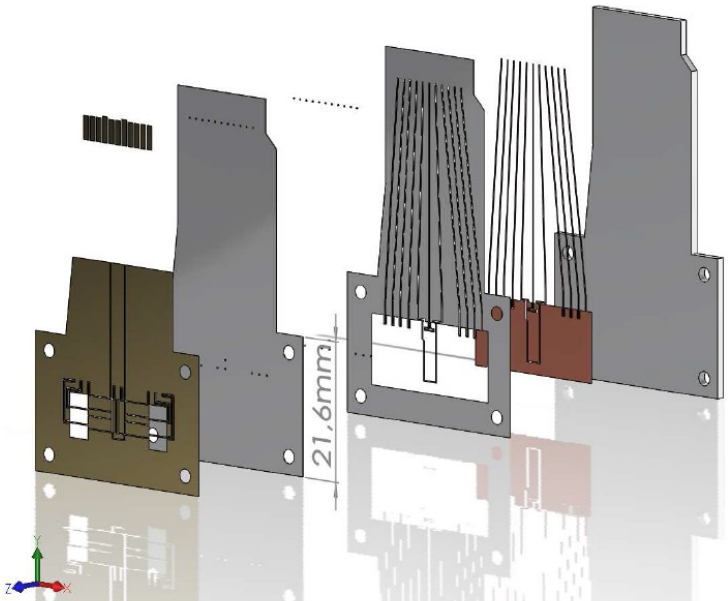


From B. Szymanski PhD thesis



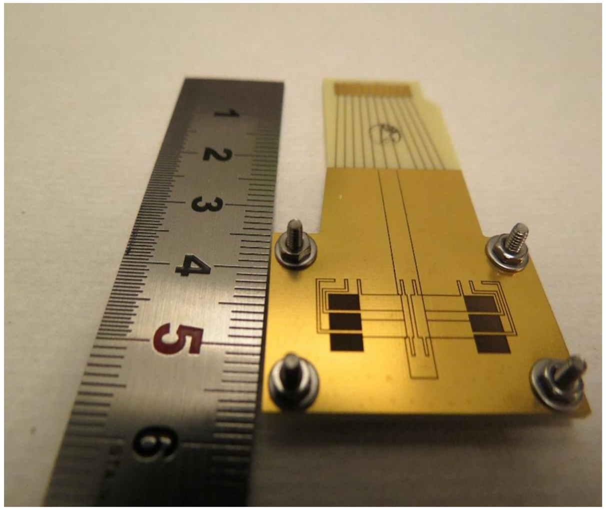
From https://aquadrupauliontrap.wordpress.com/background/

Current $^{171}Yb^{+}$ trap



Current trap version :
- Five wire geometry.
- Printed circuit.
- Substrat FR-4.
- Plug-in SD.
- Chip carrier made out of MACOR.
- DC voltage : about 5 V.
- RF voltage : about 250 Vpp.
- RF frequency : 5.6 MHz

Problems :
- Low trenches aspect ratio : wide gaps (120 µm), thin electrodes (25 µm) → $\eta = 0.2$.
- Mediocre surface quality.



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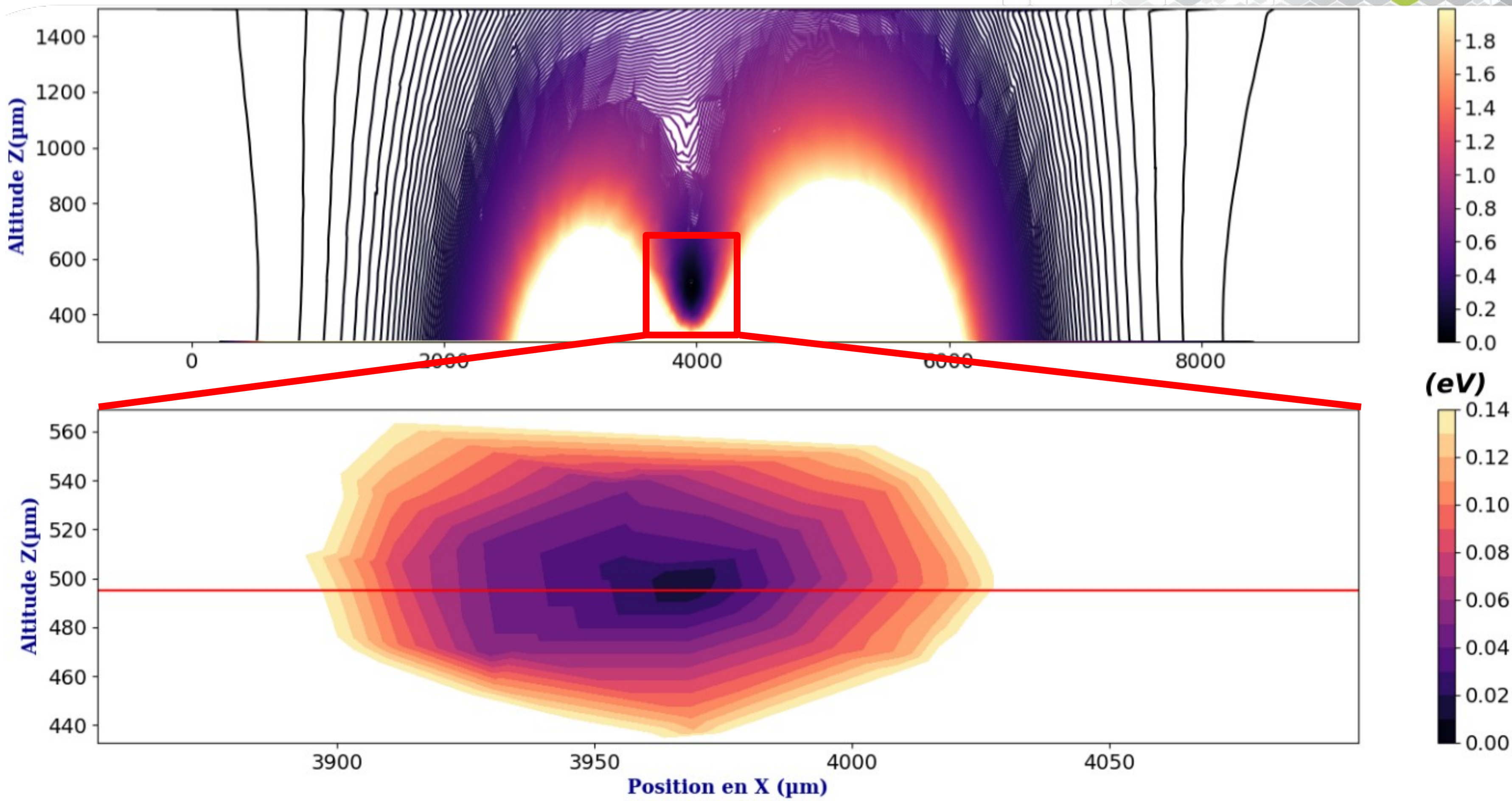
Current $^{171}Yb^{+}$ trap



- RF potential in *xz* plan, shows zero potential area at the center of the trap, 500 μm above the surface.
- RF potential shows good harmonicity as we get closer.
- Trapping frequencies are 375 kHz along *x* and 275 kHz along *z*.

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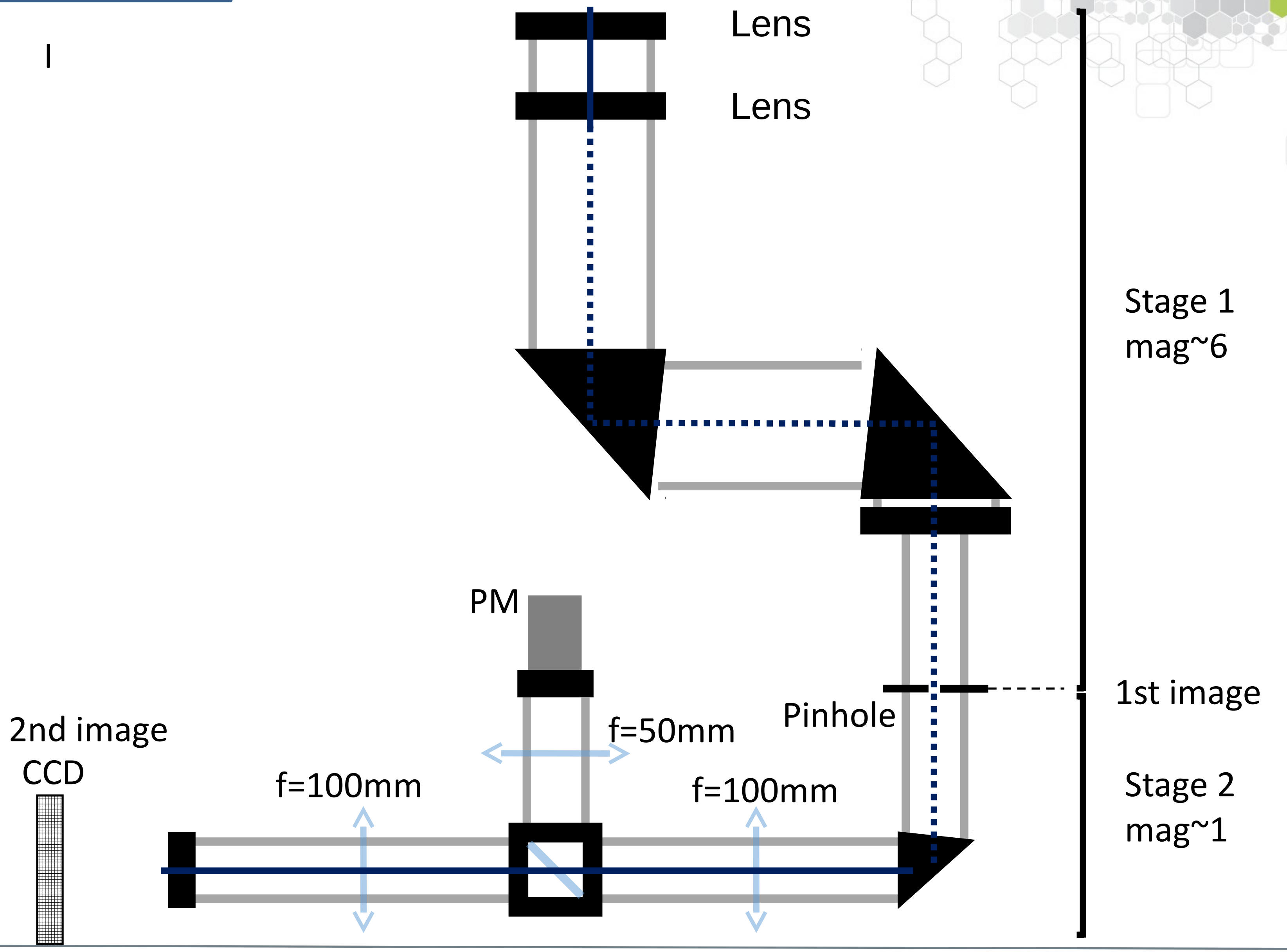
Detection

I


Lens
Lens
Stage 1
mag~6
PM
1st image
f=50mm
Pinhole
2nd image
CCD
f=100mm
f=100mm
Stage 2
mag~1

Trapped ions

We managed to trap several ions, either single ions or in Coulomb crystal configuration.

- 1 mm pinhole
- Band-pass optical filter (370 nm)
- The ability to form 1D Coulomb crystals allows to set an upper bound on temperature (10 mK)

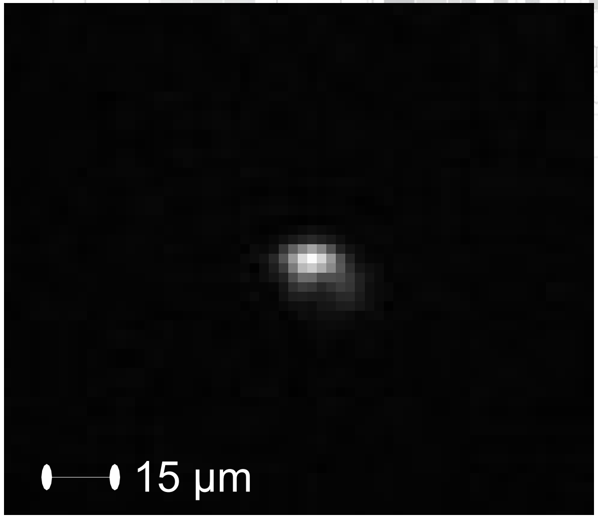


Image of a single ion taken with CCD camera.

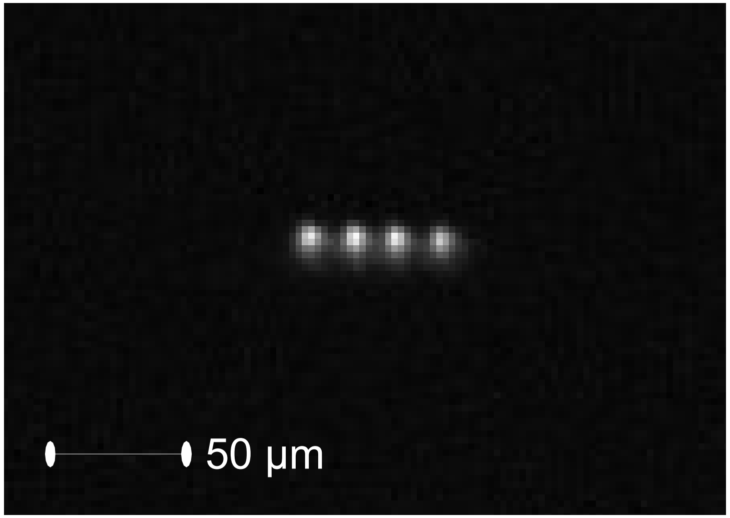
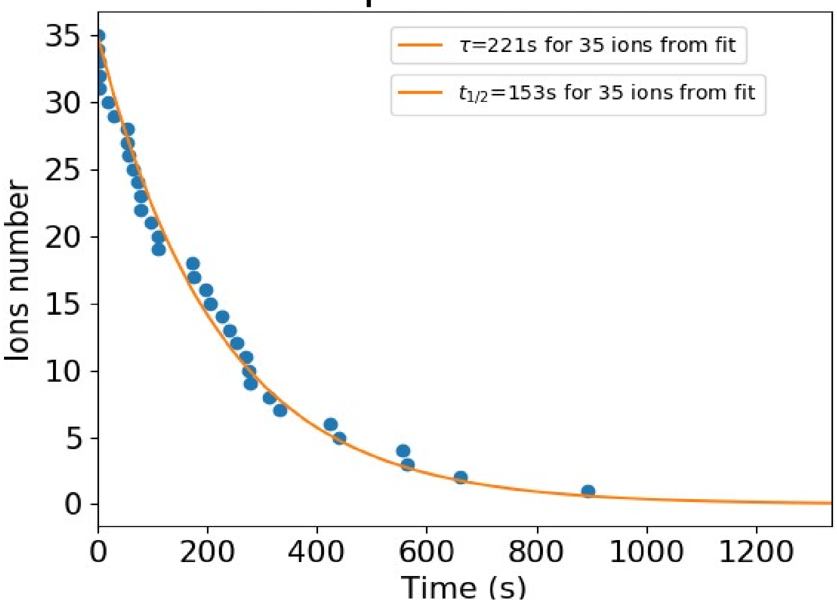


Image of a four ions Coulomb crystal taken with CCD camera.

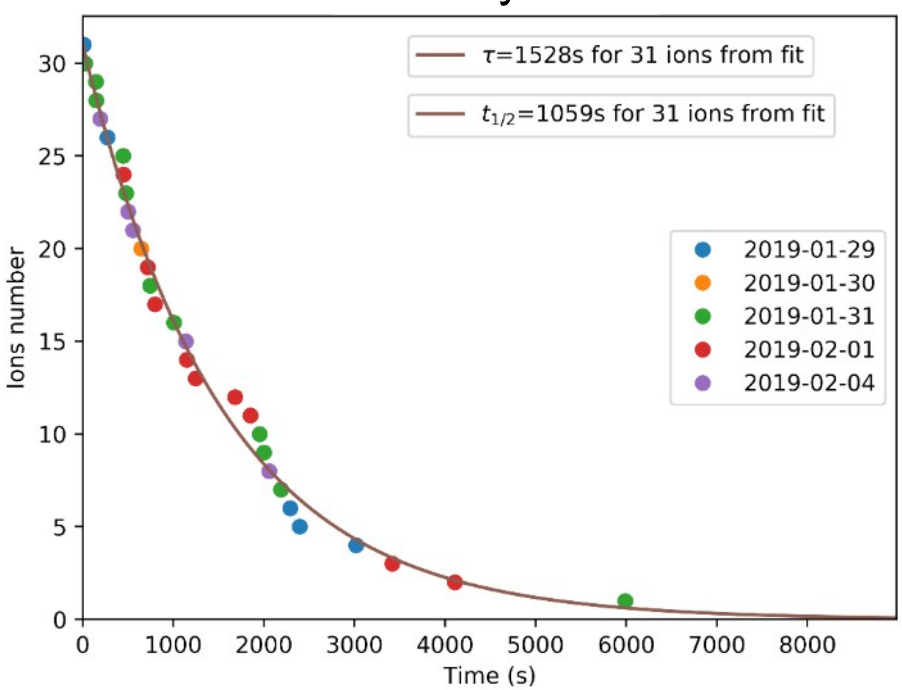
Life-times record

September 2018



- Several single ions trapped.
- Every lifetime recorded
- « high pressure » suspected to be responsible for quite short lifetimes (τ = 221 s).

January 2019



- Bake-out.
- Lower the pressure down from 3.10^{-9} to 5.10^{-10} mbars.
- Greatly enhanced lifetime, up to τ = 1528 s.

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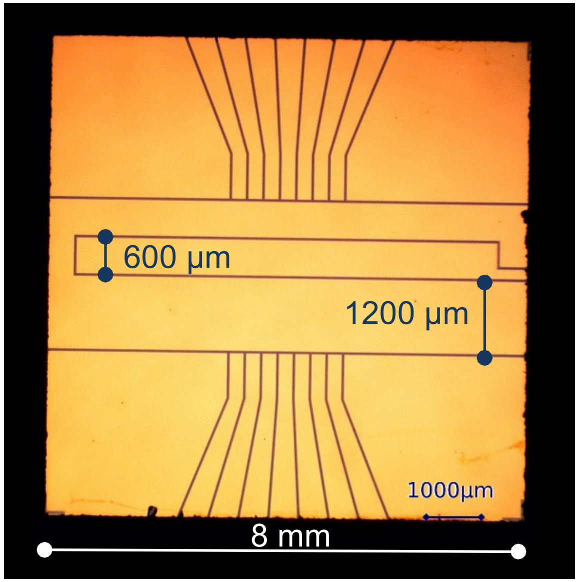
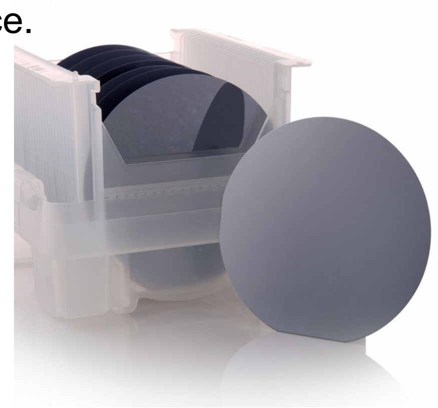
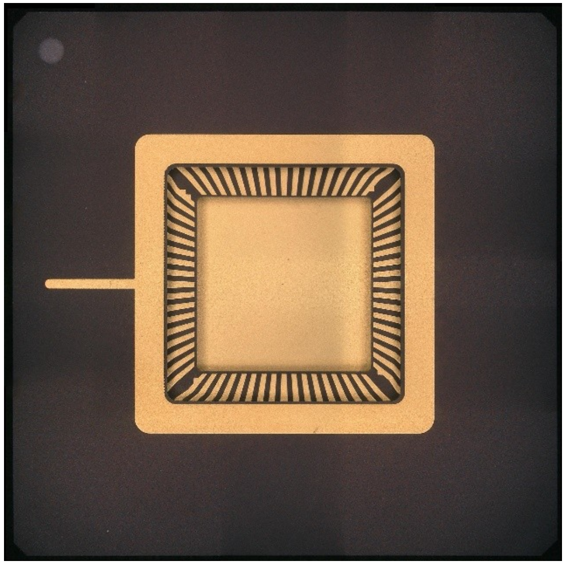
New Trap



- Went from prototype to clean trap.
- Full device is 8 x 8 mm.
- Central DC electrode is 600 µm wide.
- The RF « fork » is 600 and 1200 µm wide.
- Each DC control electrode is 250 µm wide.
- Gap: 20 µm wide, 200 µm deep → aspect ratio = 10
- Trapping distance: 650 µm above the surface.



- Wafer 4 inches.
- Si++(B)/Box/Si++(B)
- Wafer bonding with Si+ (500µm).



- Chip-carrier (Global Chip Materials).
- Ceramic UHV compatible.
- 68 connecting pins.
- Low magnetic field (≈ 100 µG) but Ni in connection pins.

Step 1 : Wafer-bonding by thermocompression

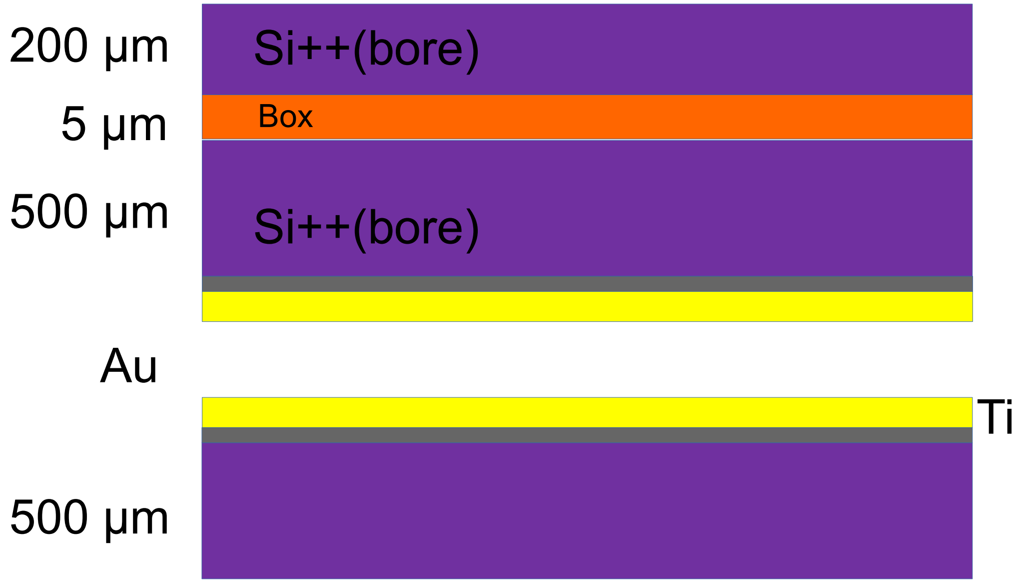
Solution to chip-carrier 1100 µm depth

- We applied a 30 nm Ti layer and a 250 nm Au layer by sputtering to the two wafers.

- Compress the wafers with a 4kN force, at low N_2 pressure (10^{-6} mbars).

- Heating up to 250°C.

- Slowly relieve the compression tool.

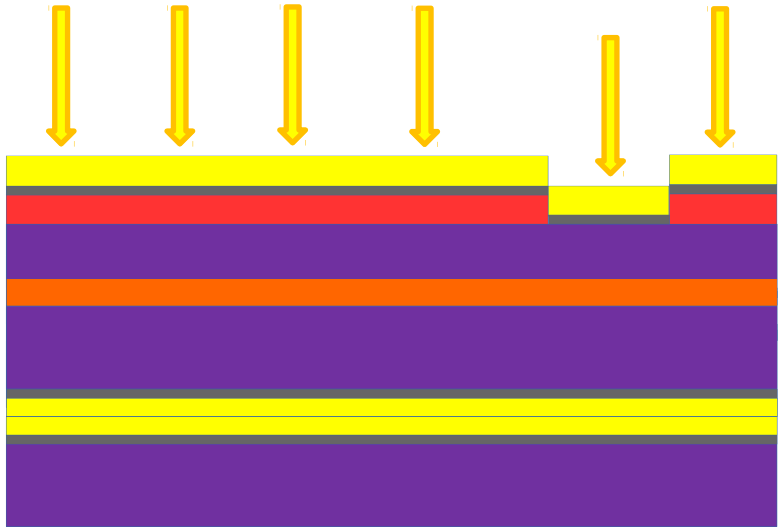


Step 2 : Gold electrode

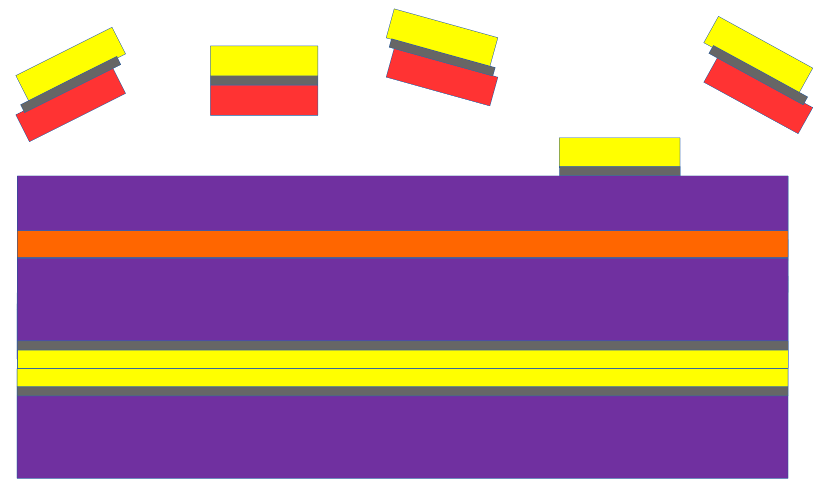
- Photolithography

Resist

- Evaporation Ti: 30 nm + Au: 250 nm



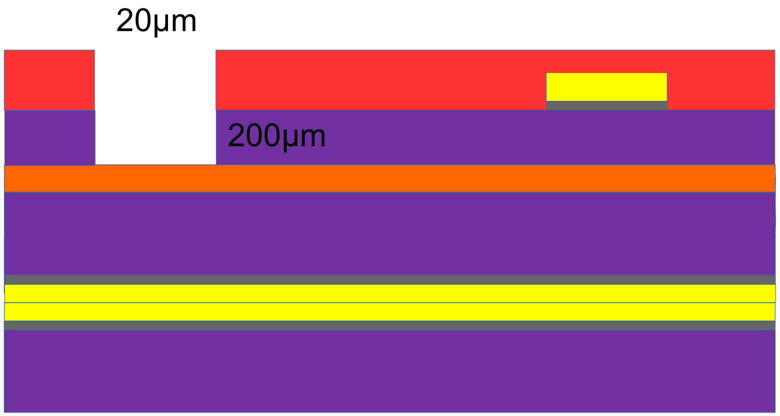
- Lift-Off.



Step 3 : DRIE

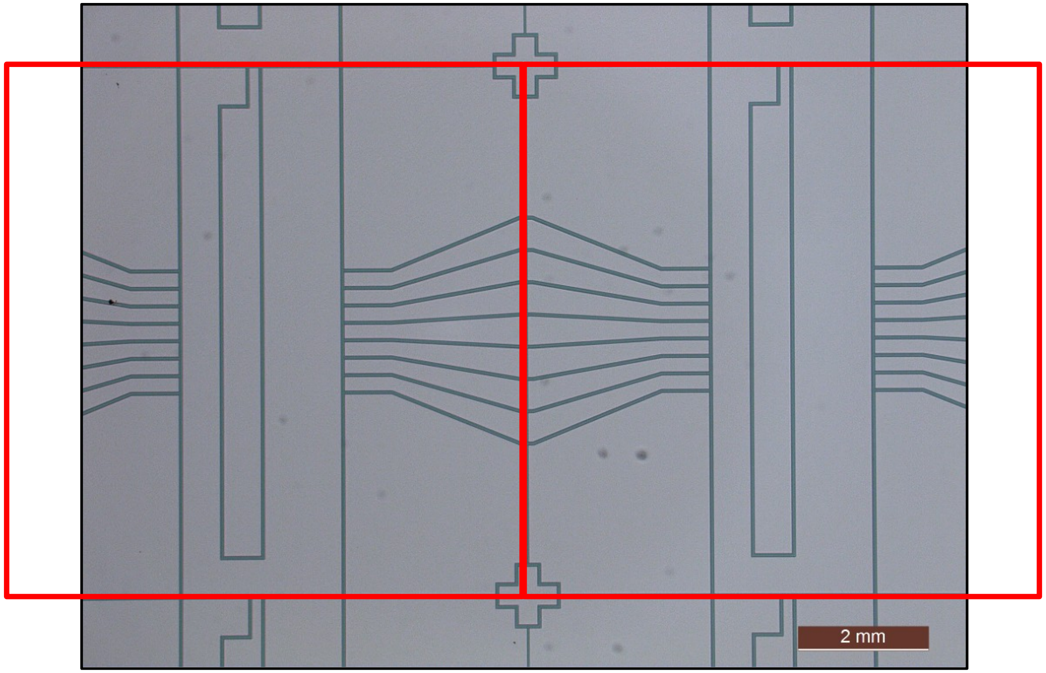
- Photolithography.

- DRIE etching.
- 20 µm wide gaps.
- 200 µm depth etching (down to the Box).
- Scalloping lowering to 100 nm or below.

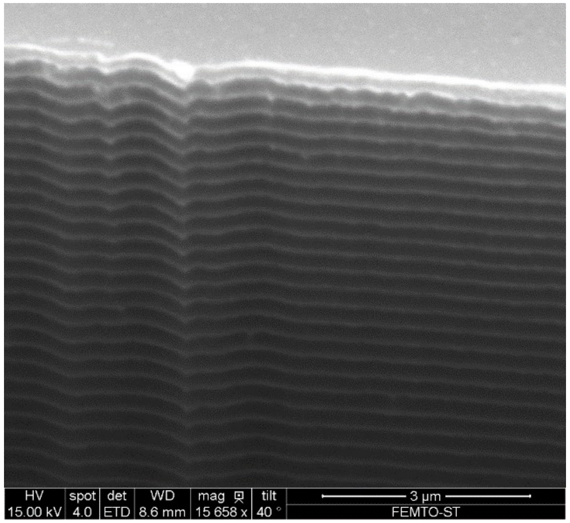


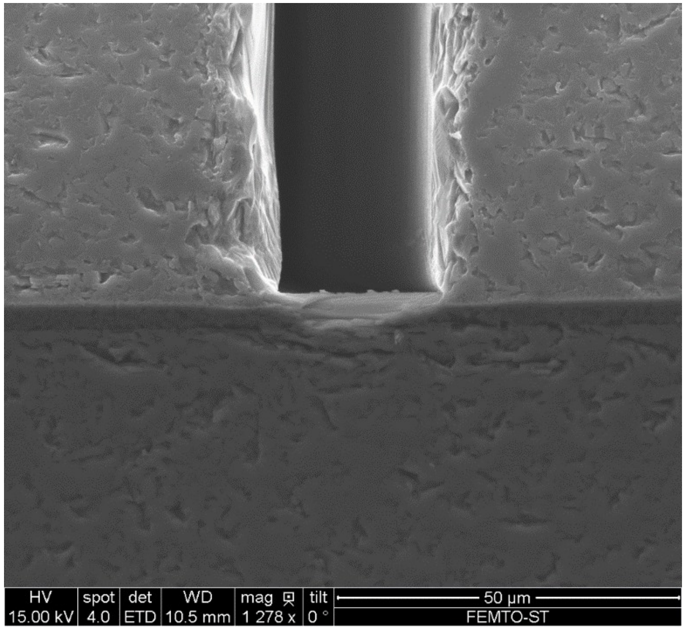
Step 4 : Packaging

- Resin layer to protect devices during saw-cutting step (300 µm width blade).
- Gluing the device to the chip carrier with H20E ultra-vacuum glue.
- Wire- bonding.
- O_2 plasma cleaning (reduce anomalous heating).
- Goes in main chamber.



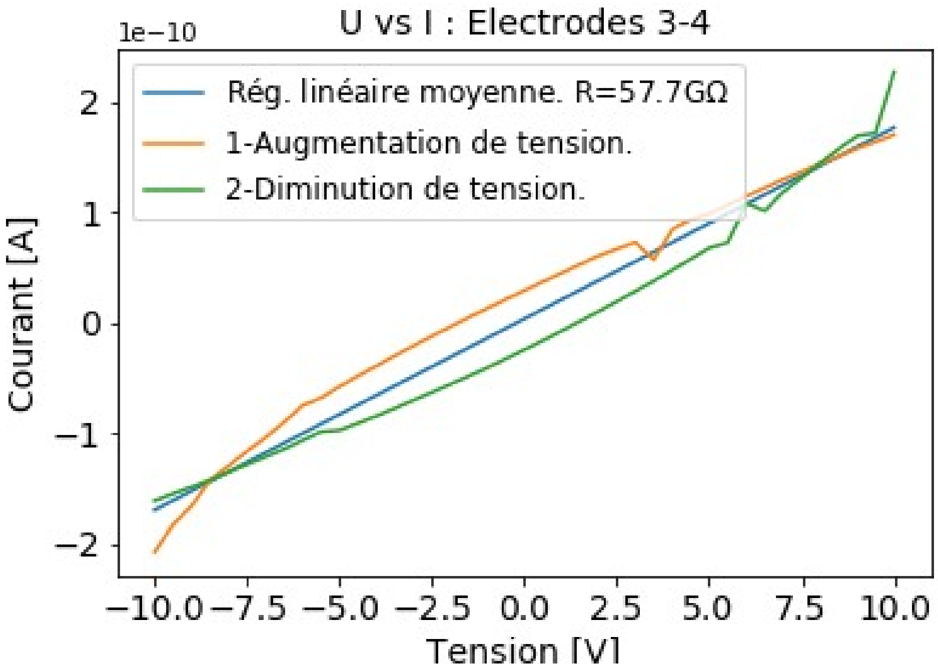
Step 4 : Packaging



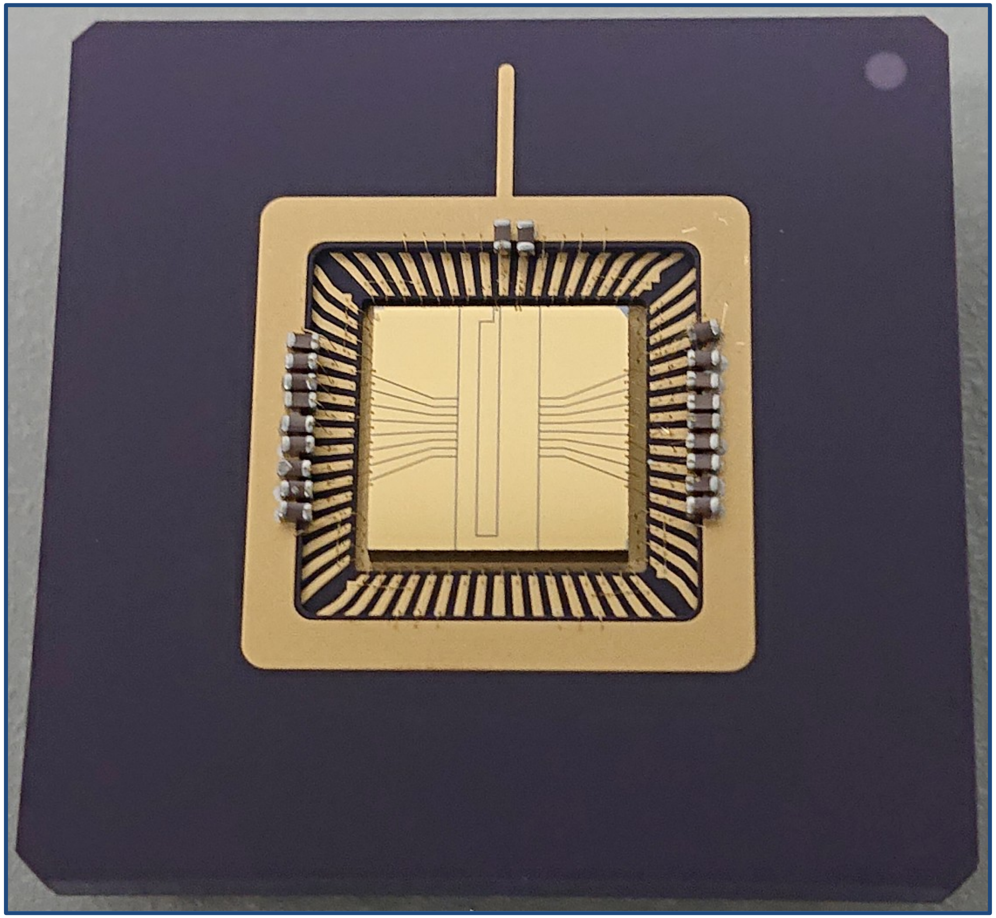


<u>Two steps verification of the isolation of electrodes:</u>

- We broke a piece of the wafer to look at the side with MEB (Plassys MEB 600).
- Using a prober, we measured the current between each pair of electrodes.



Final device



- Higher trapping distance (from 500 to 650 µm).
- No ferromagnetic materials in electrodes.
- Aspect ratio from 0.2 to 10.
- No degassing materials.
- Cleaner surface quality.

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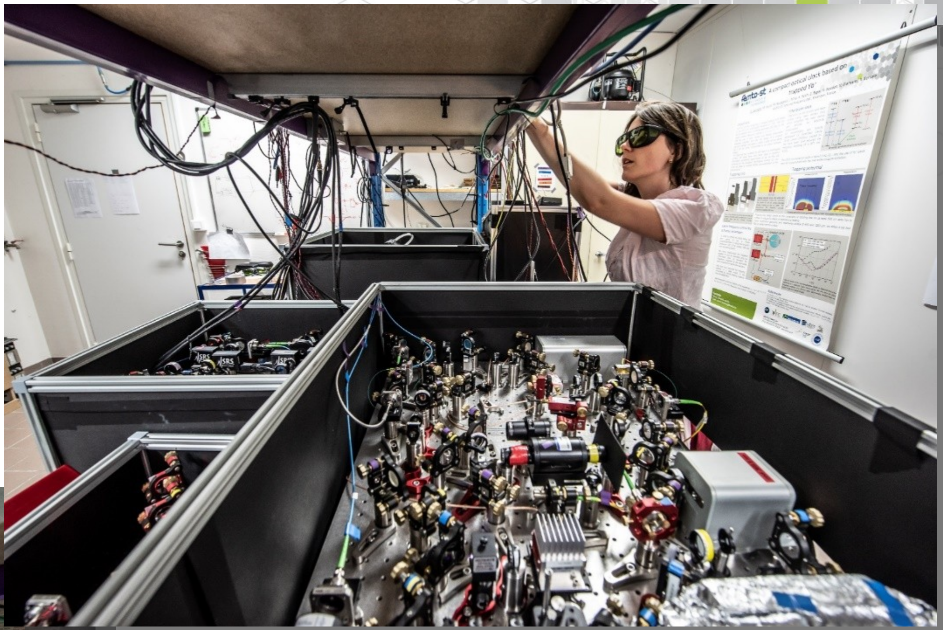
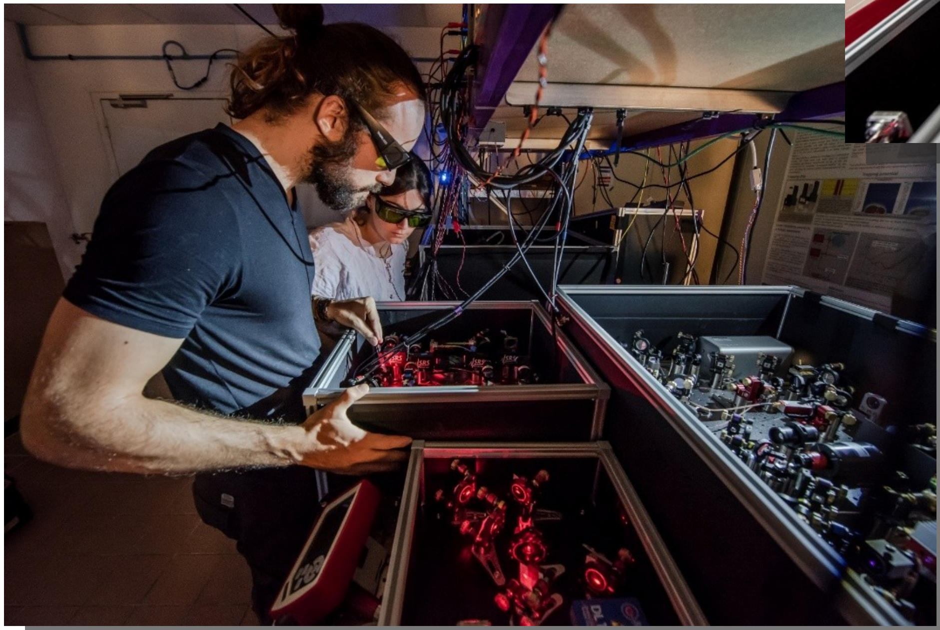
Conclusion

- First trapped ion in Besançon (05/2018)
- Fourth french ion trapper team (all in First-TF) member of the COST TIPICQA.
- Pressure low enough to allow decent life-time (atomic clock)
- Clock laser locked on a frequency comb, but will be locked on ULE cavity in the future (Avinash Kumar).
- Digital control of the experiment will be implemented soon. (Pierre-Yves Bourgeois, Bachir Achi, Jules Chatelier).
- New trap is now ready.
- Spectroscopy coming soon.

Team work

Thank you for your attention !





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Lasers set-up