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Addressed

Research Questions/Problem

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Result

Discussion an Conclusions

Current and

Caractérisation de l'instabilité des oscillateurs : étude des performances logicielles et matérielles d'un banc de mesure à base d'électronique numérique reconfigurable

A. C. Cárdenas-Olaya, C. E. Calosso, P.-Y. Bourgeois, A. Hugeat, J.-M Friedt, E. Rubiola









June 22, 2017

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Research Context and Motivation

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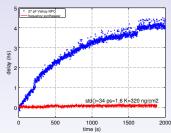
Discussion ar

Current and Future Worl

Why Digital Instrumentation?

Comparison between digital and analog implementation:

Sampling Time Generator for stroboscopic measurement.



Ground Penetrating Radar (GPR)

- Analog components highly dependent on environmental factors, drift, aging and tuning.
- Digital implementations -Software Defined Radio (SDR) techniques.

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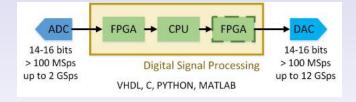
Plan of Work

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Discussion a

Current and Future Work

General Purpose Digital Instrument Structure



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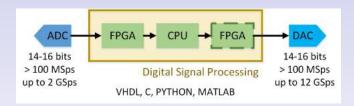
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General Purpose Digital Instrument Structure



- **Stability:** Once the code or configuration algorithm (FPGA) is working it will work in the same way over time.
- Reconfigurability: Modifications during development can be performed only by changing the algorithm (CPU or FPGA configuration). Good for testing new approaches and techniques.
- **Flexibility:** Reproducible systems just by changing parameters (gains, coefficients, data resolution, etc.).

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Current and

Replacing Analog with Digital Introduces Some New Challenges

- Discrete Time: Limited Observation Bandwidth
- Aliasing
- Quantization
- Sample Representation: Integer, Fixed Point, Floating Point

That could be taken as opportunities for the development of new approaches as: *Stroboscopic Measurement*

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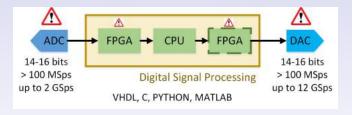
Plan of Work/ Methodology

Recul

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Current and Future Work

Understanding Hardware Limitations: Characterization of Front-End Hardware



Available noise information of the components at frequency offsets far from the carrier.

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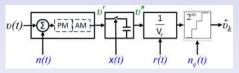
Discussion ar Conclusions

Current and

Model for ADC Phase and Amplitude Noise Characterization

Extract and discriminate the different noise sources.

- Predict effects of ADC noise on the digital system performance.
- Characterization for time and frequency metrology applications.



- n(t): Addtive Noise of Input Stage.
- x(t): Aperture Jitter.
- r(t): Voltage Reference Noise.
- $n_q(t)$: Quantization Noise o high resolution ADCs

$$S_{\varphi,s}(f) = rac{1}{V_0^2} S_{n_{\varphi},s}(f) + 4\pi^2
u_0^2 S_{x,s}(f)$$
 $S_{\alpha,s}(f) = rac{1}{V_0^2} S_{n_{\alpha},s}(f) + S_{r,s}(f)$

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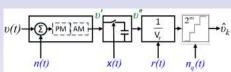
Discussion :

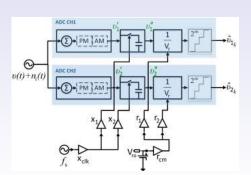
Current and

Model for ADC Phase and Amplitude Noise Characterization

Extract and discriminate the different noise sources.

- Predict effects of ADC noise on the digital system performance.
- Characterization for time and frequency metrology applications.
- Differential applications ⇒ Common noise rejection.





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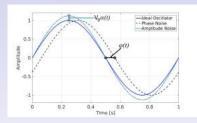
Discussion ar Conclusions

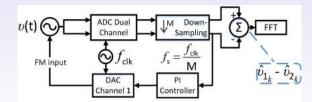
Conclusions

Method for the Extraction of ADCs Noise Components

$$S_{\varphi,s}(f) = \frac{1}{V_0^2} S_{n_{\varphi},s}(f) + 4\pi^2 \nu_0^2 S_{x,s}(f)$$

$$S_{\alpha,s}(f) = \frac{1}{V_0^2} S_{n_\alpha,s}(f) + S_{r,s}(f)$$





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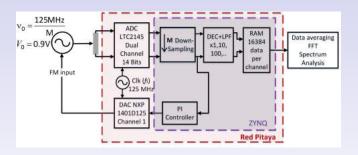
Plan of Work/ Methodology

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Discussion a Conclusions

Current and Future Wor

Implementation of the Method Proposed



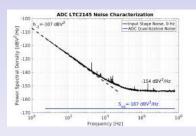
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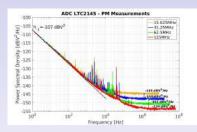
- 14-bit dual channel ADC, 125 MSps
- 14-bit dual channel DAC, 125 MSps
- System On Chip (SoC) = ARM processor + FPGA

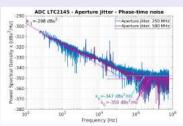
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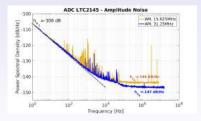
Results

ADC Noise Characterization









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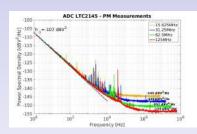
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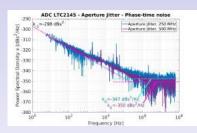
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Current an

ADC Noise Characterization





Parameter

ADC LTC2145 Common Mode

$$\begin{array}{|c|c|c|}\hline h_0 B = \frac{b_{s_0} f_s V_0^2}{2} & \sqrt{h_0 B} = 159 \ \mu V_{rms} \\ \hline h_{-1} = b_{s_{-1}} V_0^2 & \sqrt{h_{-1}} = 4.5 \ \mu V \\ \hline J^2 = k_0 \frac{f_s}{2} & J = 25 \ \mathrm{fs_{rms}} \\ \hline k_{-1} & \sqrt{k_{-1}} = 1.3 \ \mathrm{fs} \\ \hline \end{array}$$

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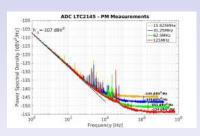
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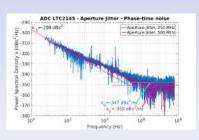
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Comparing ADC LTC2145 Phase Noise Results





Parameter	ADC	Generic	Amplifier
Phase Noise	LTC2145	Mixer	OPA354A
$\sqrt{\mathrm{h}_0}$	$10~{ m nV}/\sqrt{ m Hz}$	$3 \text{ nV}/\sqrt{\text{Hz}}$	$6.5~\mathrm{nV}/\sqrt{\mathrm{Hz}}$
	B = 250 MHz	5 - 10 MHz	$B = 250 \; MHz$
$\sqrt{h_{-1}}$	4.5 μV	0.1 μV	1.9 μV

For comparison with amplifiers and mixers.

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Discussion and Conclusions

- The model and the method can be reproduced for the characterization of any ADC architecture.
- Working with high resolution ADCs reduces the effect of the quantization noise. At high speed and high input amplitude a better performance is achieved.
- The ADC noise is dominated by the noise of the input stage that is equally distributed between amplitude and phase noise.
- Even if this component could limit low noise measurements, the characterization brings key information for noise rejection techniques.

A. C. Cárdenas-Olaya, E. Rubiola, J.-M., Friedt, P.-Y. Bourgeois, M. Ortolano, S. Micalizio, C. E. Calosso, *Noise characterization of analog to digital converters for amplitude and phase noise measurements*. Accepted for publication in Rev. Sci. Instrum.

(Available at: http://jmfriedt.free.fr/rsi_ADC_Characterization.pdf)

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Current and Future Work

Current and Future Work

- Study of other critical blocks: DAC and PLL.
- Noise characterization of other platforms with different architectures and features.
- This project is part of GoDigital group that is currently working on:
 - Arithmetic analysis and scheduling of digital processing and
 - On implementation of applications for time/frequency metrology based on digital instrumentation.



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